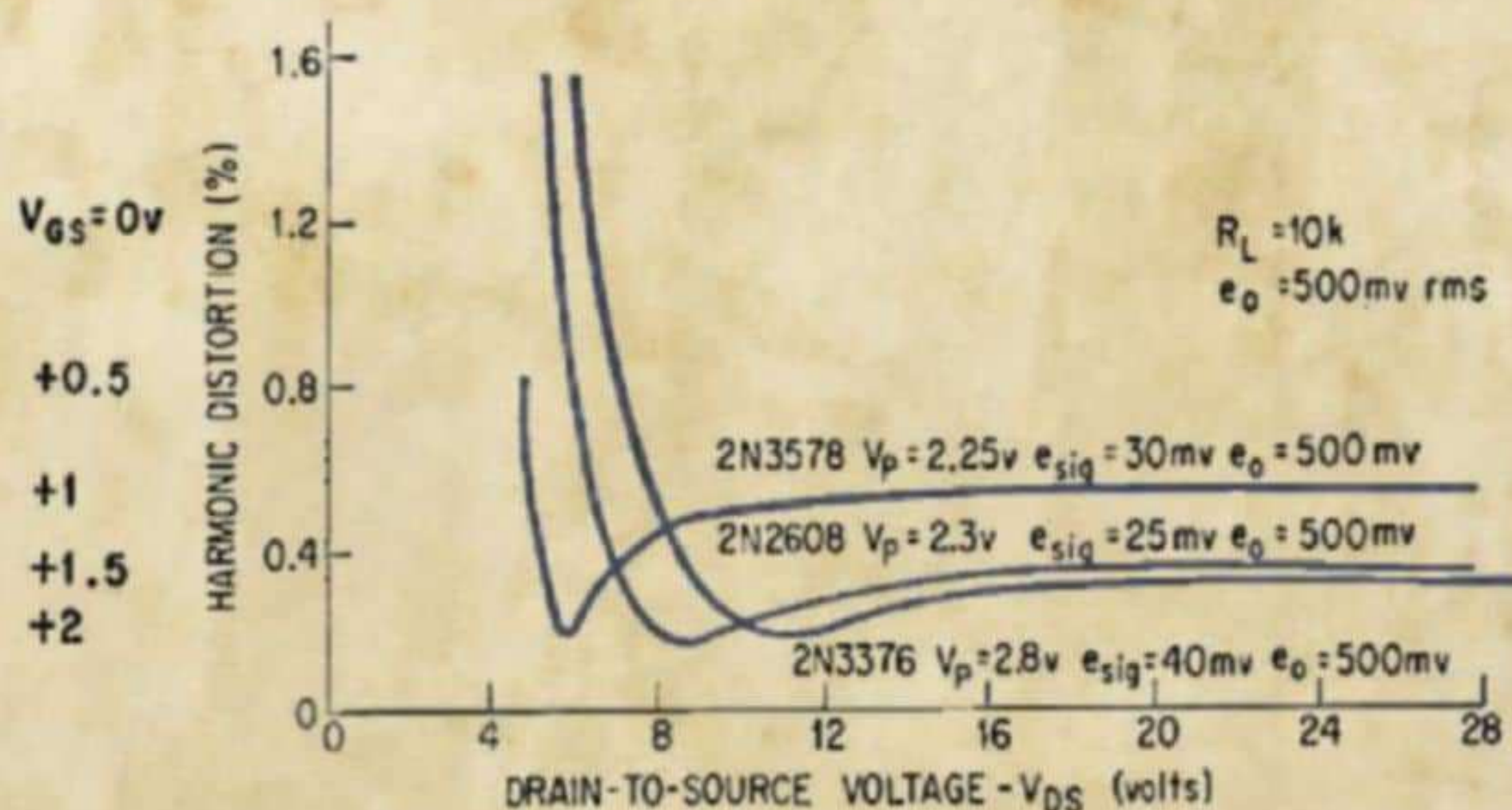
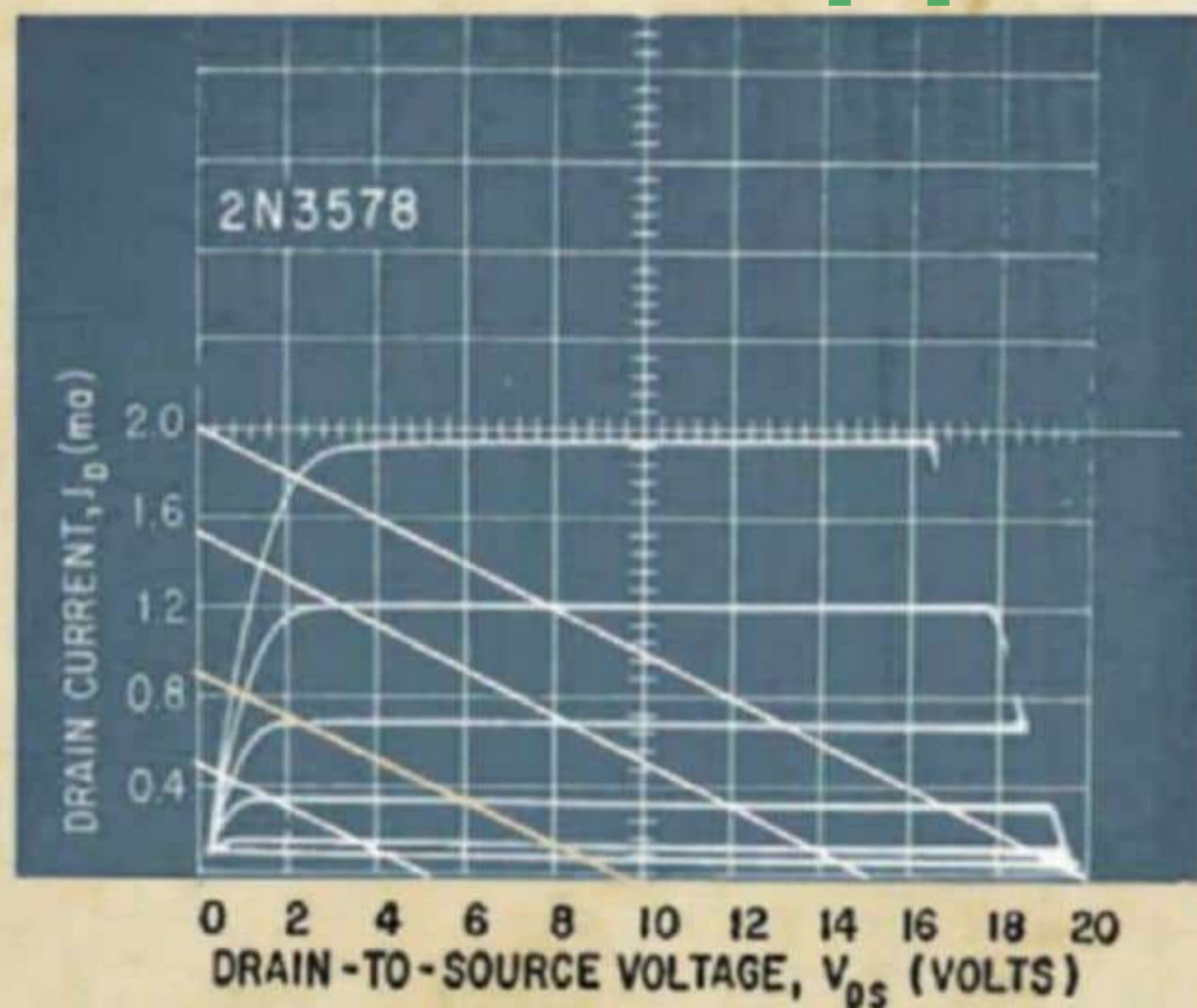


# JFETs in the Variable-Resistance Mode and their Application in Audio Circuits



By  
**Dimitri Danyuk**

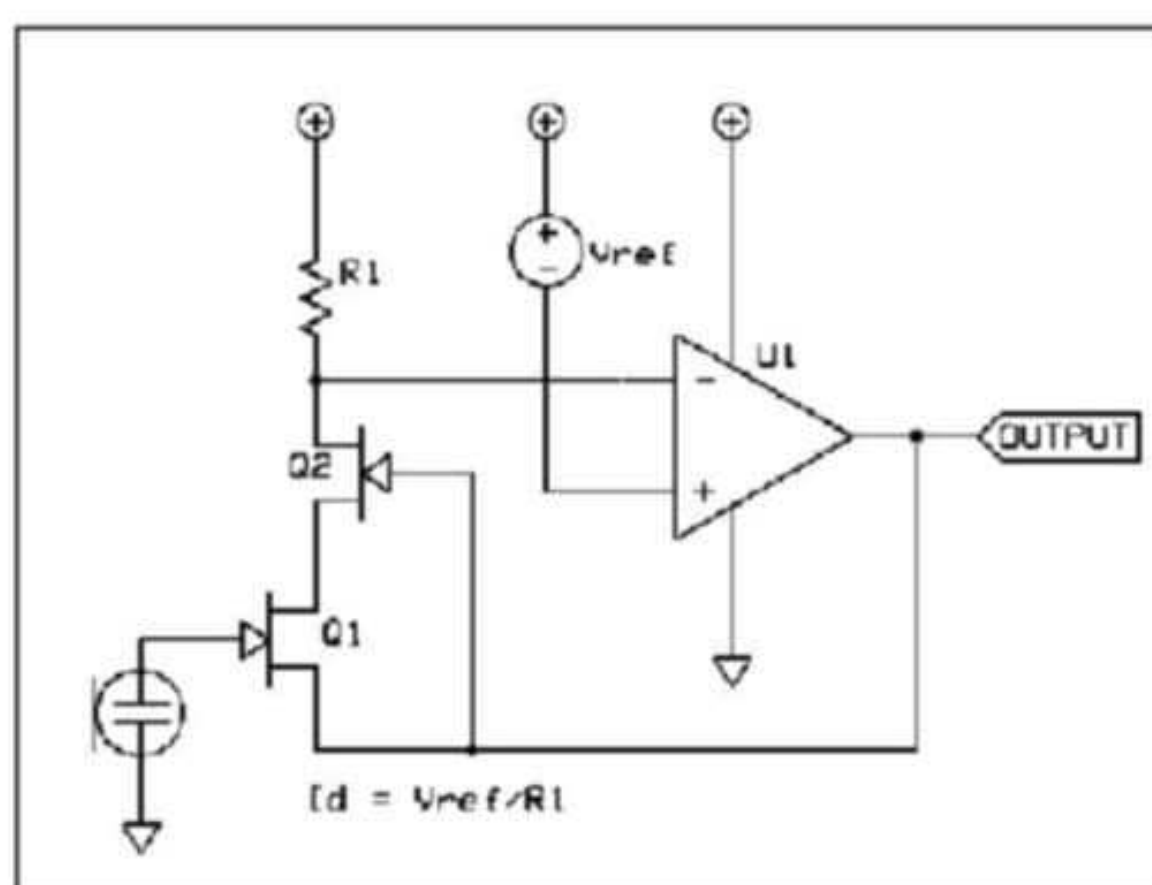
This article explores the variable-resistance mode of JFET operation and describes a practical circuit, built around JFETs in the variable-resistance mode with a drain load resistor. The circuit is applied in a complete phono preamp design in transconductance mode.

The junction-gate field-effect transistor (JFET) has two distinct modes of operation: the variable-resistance mode (resistive mode, Ohmic region, or triode region) and the saturation (pinch-off or pentode) mode. In the resistive mode the JFET behaves like a resistor whose value is controlled by the voltage between gate and source  $V_{gs}$ . In the saturation mode an increase in  $V_{ds}$  does not result in a correspondent increase in  $I_d$ , and the output characteristic flattens out. The channel is heavily constricted with most of the drain-source voltage drop occurring along the narrow and therefore high-resistance part of the channel. Let's start with the variable-resistance mode of operation.

## JFETs in the Variable-Resistance Mode

Twelve years ago, I designed an impedance converter for condenser microphones for a high-end microphone manufacturer. Condenser microphone capsules have low capacitance (10pf to 80pF typically) and should be loaded at a very high impedance. An

Figure 1: Impedance converter for a condenser microphone



impedance converter (or buffer) is used to match the impedance of the microphone capsule to the input impedance of the recording device together with the long cable.

The JFET source follower is the simplest form of the impedance converter. It can be improved by adding a cascode and the output stages to the JFET follower, as shown in **Figure 1**. The cascode device reduces the input capacitance while the output stage improves the output current capability of the JFET follower. According to the handbooks, the pinch-off voltage for the upper device should be high enough to keep the lower JFET in the saturation region.

The cascode JFET Q2 works as a load for a lower JFET Q1, and voltage at the drain of Q1 follows the voltage on the source of Q1. This means that Q2 provides a low input resistance to Q1 and the gate to drain capacitance of Q1 is bootstrapped.

I tested the circuit, shown in Figure 1 with different cascode devices. The typical graph of my measured total harmonic distortion plus noise (THD+N) is shown in **Figure 2**.

Distortion in the circuit shown in Figure 1 becomes lower with lower pinch-off voltage of the cascode JFET and lower voltage between source and drain of the input JFET. That was counterintuitive, but I decided to stop and use the cascode device that gave me the lowest distortion. Later I noticed the app note by Alex Nikitin on similar cascode behavior and I allowed myself to spend some time to satisfy my curiosity.

James Sherwin investigated distortion in simple common source stages. The gain equation of the common source stage is  $A = G_{fs}(R_L + 1/G_{os})$ , where  $G_{fs}$  is the JFET forward transconductance,  $R_L$  is the load and  $G_{os}$  is the output conductance. The output



conductance  $G_{os}$  is the ratio of change in drain current  $I_d$  to a change in voltage between drain and source  $V_{ds}$ .

Transconductance  $G_{fs}$  increases with drain current  $I_d$ , and the output transconductance  $G_{os}$  also increases with  $I_d$ . Moreover, the output transconductance  $G_{os}$  increases with reduced  $V_{ds}$ . At some value of the drain current  $I_d$  and drain to source voltage  $V_{ds}$  the change in the  $G_{fs}$  can be partially offset by the change in  $G_{os}$  (or together in  $R_L$  and  $G_{os}$ ). In effect, the distortion produced by the nonlinear  $G_{fs}$  can be compensated by distortion produced by the nonlinear  $G_{os}$ . This cancellation of two distortion sources produces a point with minimum distortion.

The cascode device works as a common gate stage. The input resistance of the common gate stage is equal to  $1/G_{fs}$  and it acts as a load resistor  $R_L$  for the input JFET. Let us have a look at the cascode characteristics shown in **Figure 3**.

The small signal transfer function for the JFET at a given DC conditions may be written as a Taylor series power expansion:

$$I_d = \frac{1}{1!} G_{fs} v_{sig}^2 + \frac{1}{2!} \frac{\partial G_{fs}}{\partial V_{gs}} v_{sig}^2 + \frac{1}{3!} \frac{\partial^2 G_{fs}}{\partial V_{gs}^2} v_{sig}^3 + \dots + \frac{1}{n!} \frac{\partial^{n-1} G_{fs}}{\partial V_{gs}^{n-1}} v_{sig}^n$$

$$v_{sig} = A_{sig} \sin \omega t$$

The first term  $\frac{1}{1!} G_{fs} v_{sig}$  represents the fundamental,

the second term  $\frac{1}{2!} \frac{\partial G_{fs}}{\partial V_{gs}} v_{sig}^2$  represents DC offset plus

the second harmonic of fundamental  $\left( A_{sig} \sin^2 \omega t = \frac{A_{sig}}{2} (1 - \cos \omega t) \right)$ .

Having a look at the cascode characteristics (Figure 3), it is easy to observe an inflection point on the cascode transfer curve ( $I_d$  is about 1.8mA and  $V_{gs}$  is about -0.9V). At this point the curvature of the smooth curve changes sign, the curve shape changes from convex to concave. For a smooth curve an inflection point is a point on the graph at which the second derivative has an isolated zero and changes sign.

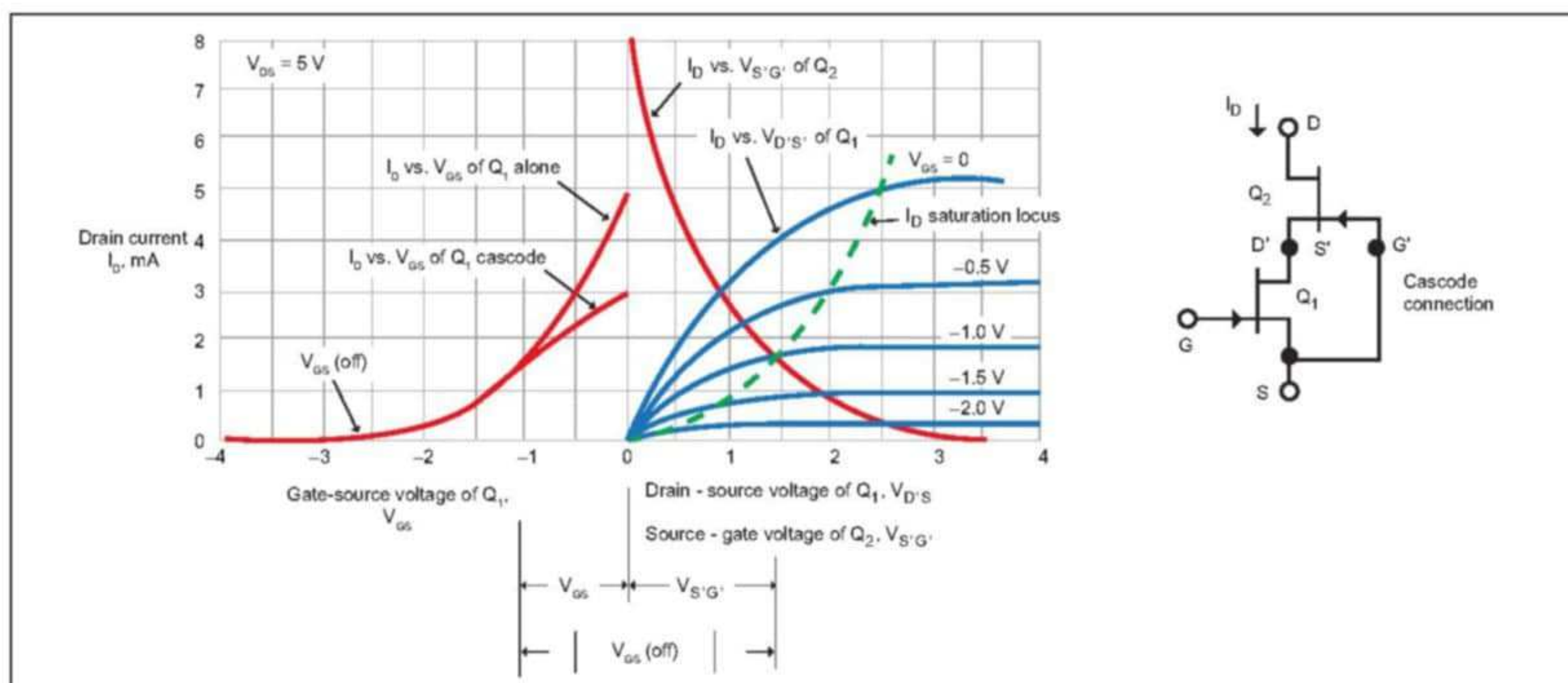


Figure 3: Cascode characteristics (from *Designing with Field-Effect Transistors*, ed. by A.D. Evans, McGraw-Hill, New York, 1981)

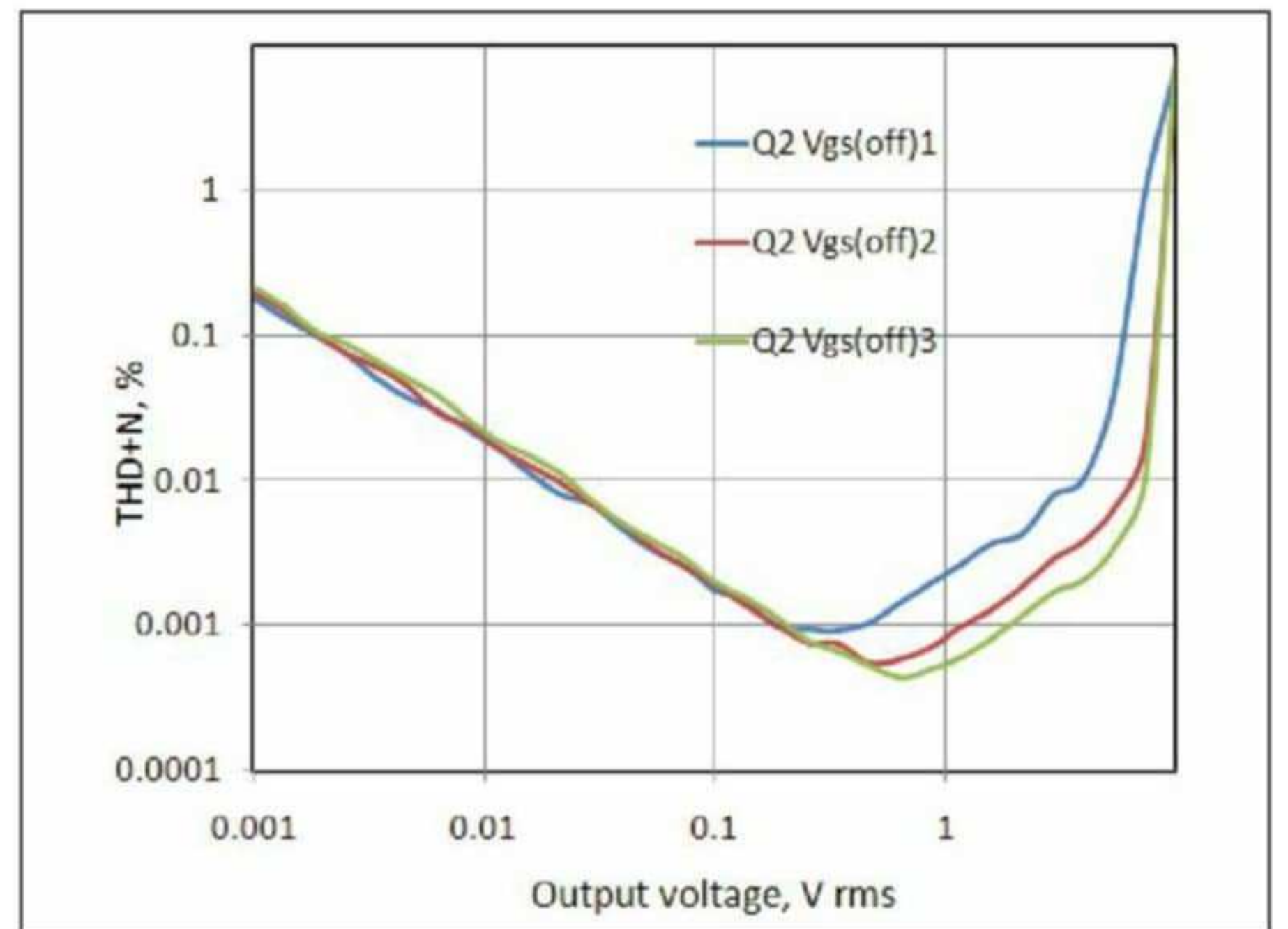


Figure 2: Total harmonic distortion plus noise for the circuit shown in Figure 1 with different cascode JFETs.  $V_{gs}(\text{off})$  is the pinch-off voltage of the cascode JFET Q2,  $Q2 V_{gs}(\text{off})1 > Q2 V_{gs}(\text{off})2 > Q2 V_{gs}(\text{off})3$ .

As  $G_{fs} = \frac{\partial I_d}{\partial V_{gs}}$  the second term can be rewritten as  $\frac{1}{2!} = \frac{\partial^2 I_d}{\partial V_{ds}^2} v_{sig}^2$ .

At the inflection point  $\frac{\partial^2 I_d}{\partial V_{ds}^2}$  is equal to zero, the second harmonic distortion, associated with the second term is zero and we can expect that the THD will reach minimum value in the vicinity of the inflection point, by operating on the most linear portion of the transfer curve.

To check the distortion behavior of the different JFETs in cascode configuration I assembled the simple circuit shown in **Figure 4**. Current source  $I$  sets the operating current for the input JFET Q1 and for cascode JFET Q2; a floating DC voltage source sets  $V_{ds}$  for the input device.

I measured dozens of JFETs and MOSFETs with this and the following circuit but will only share data for CPH3910 JFET (**Figure 5**) to save space. Results obtained with other devices are similar. There is a distortion minimum for each value of drain current. The distortion minimum becomes deeper and wider with drain current.

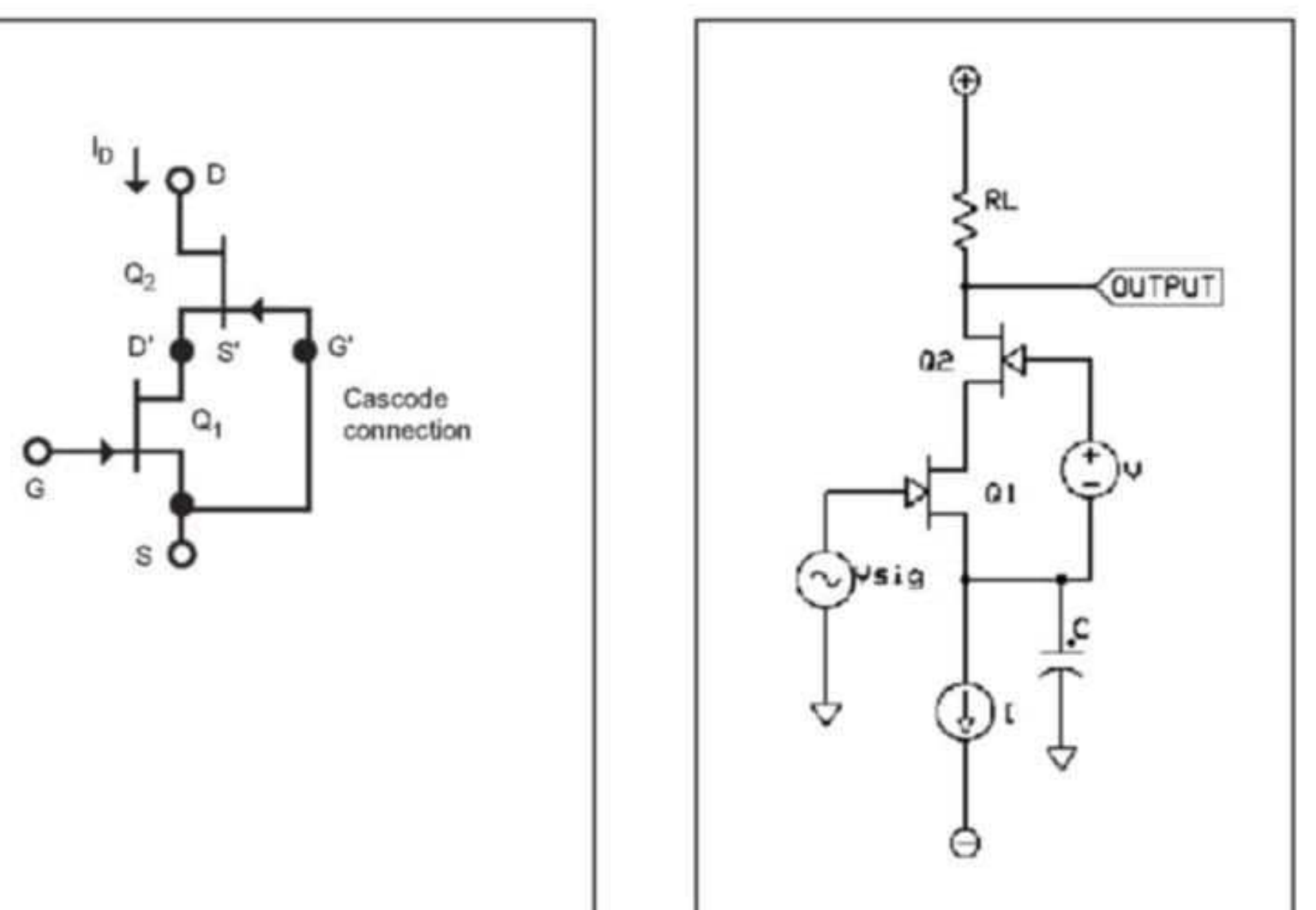


Figure 4: Circuit for cascode distortion measurement with variable  $V_{ds}$  of the input JFET



My next step was to determine the role of the cascode device. Does the nonlinearity of its input resistance play the leading role in changing the curvature of the transfer function and corresponding distortion reduction? To answer this question, I assembled the circuit shown in **Figure 6**. The cascode device is replaced with resistor connected in series with the drain terminal of the input JFET. The op-amp together with MOSFET Q2 maintains the stable voltage on the other side of the drain resistor being equal in value to floating DC voltage source  $V$ . The input JFET drain current passes through MOSFET Q2 to load resistor  $R_L$ .

**Figure 7** shows the distortion for the JFET with drain resistor. Again, you can notice distortion

Figure 5: THD+N for CPH3910 JFET with variable  $V_{ds}$  of the input JFET. Cascode JFET is also CPH3910. The input signal is 10mV rms.

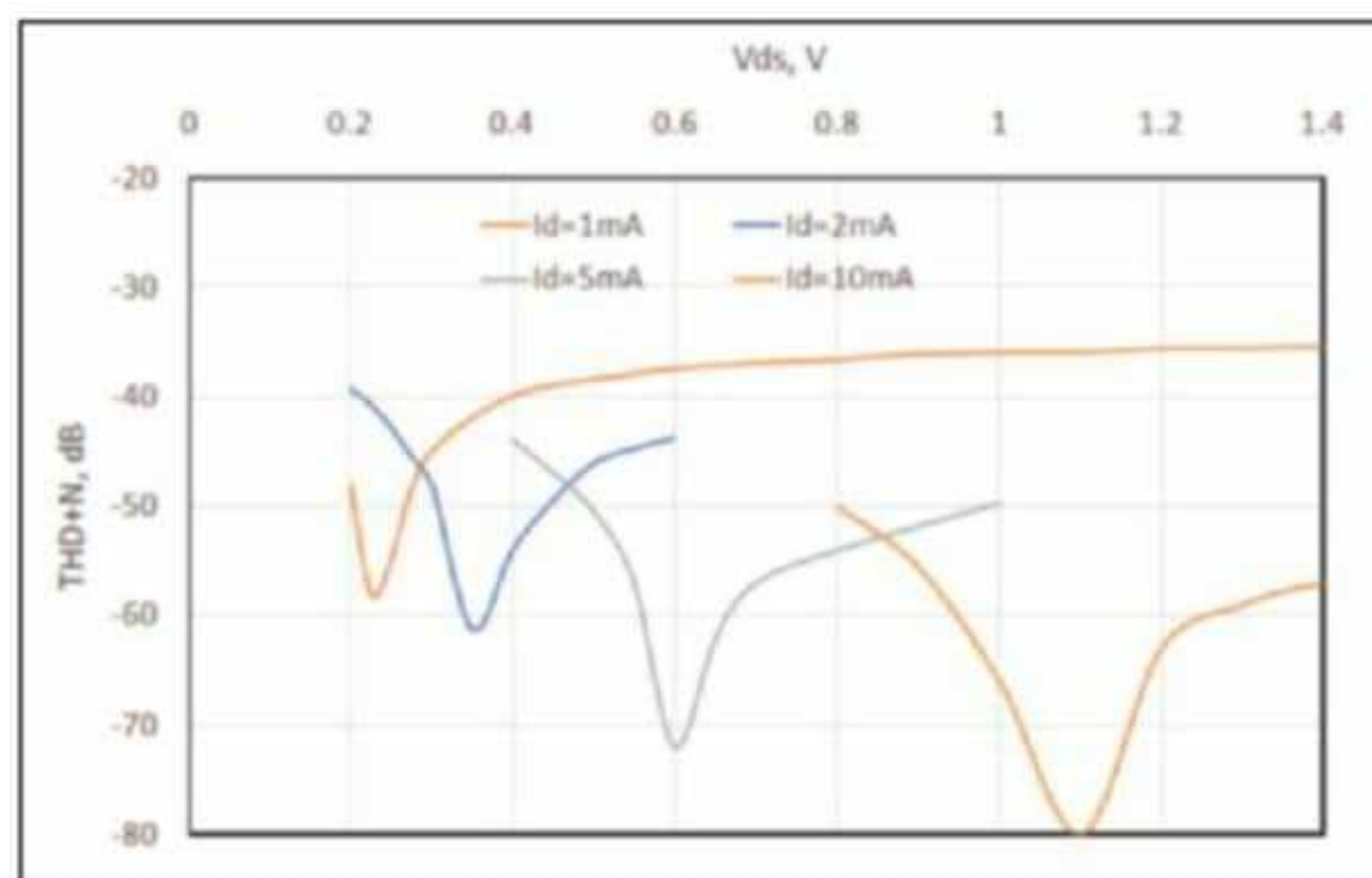


Figure 6: Circuit for JFET distortion measurement with variable  $V_{ds}$

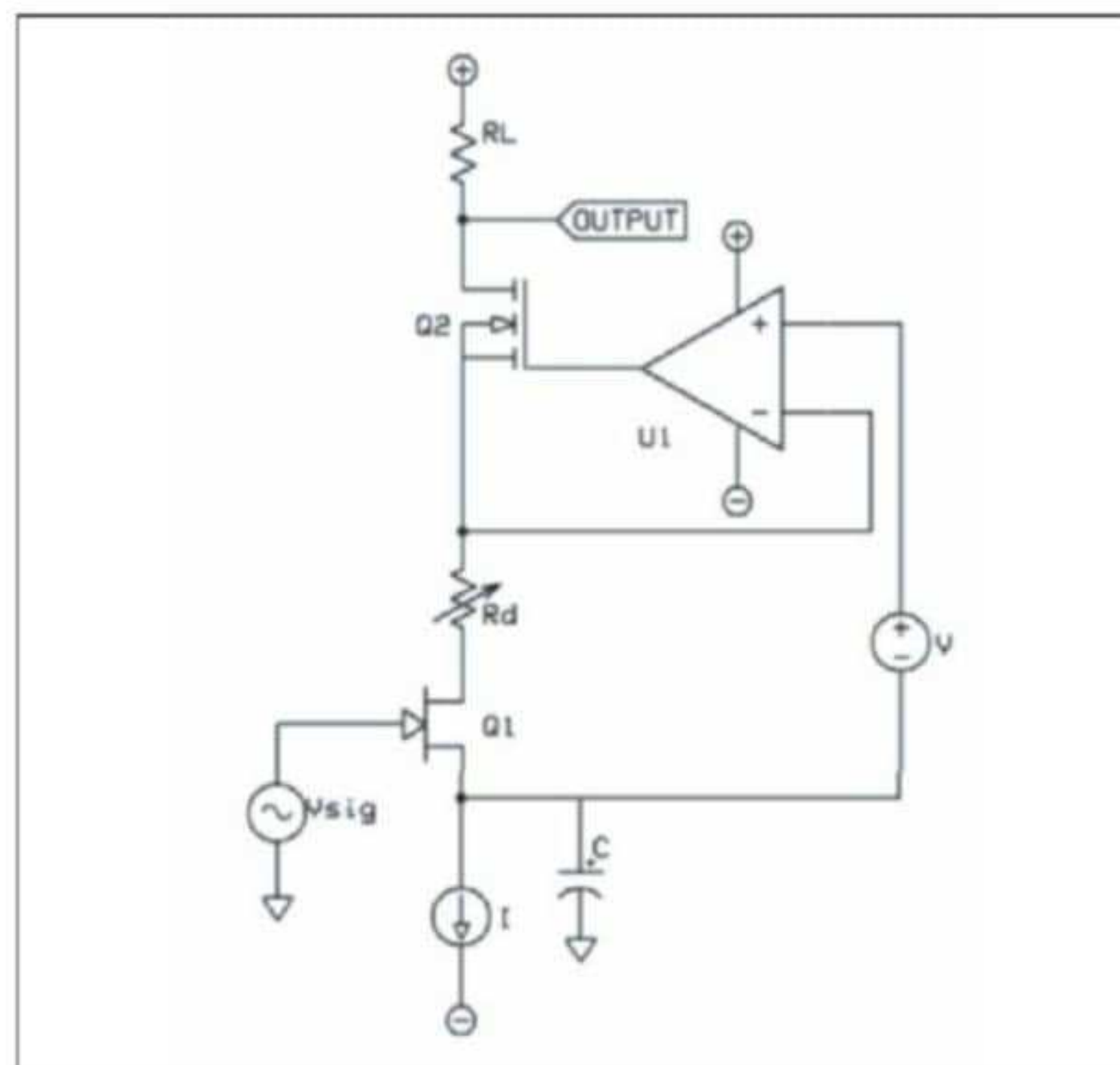
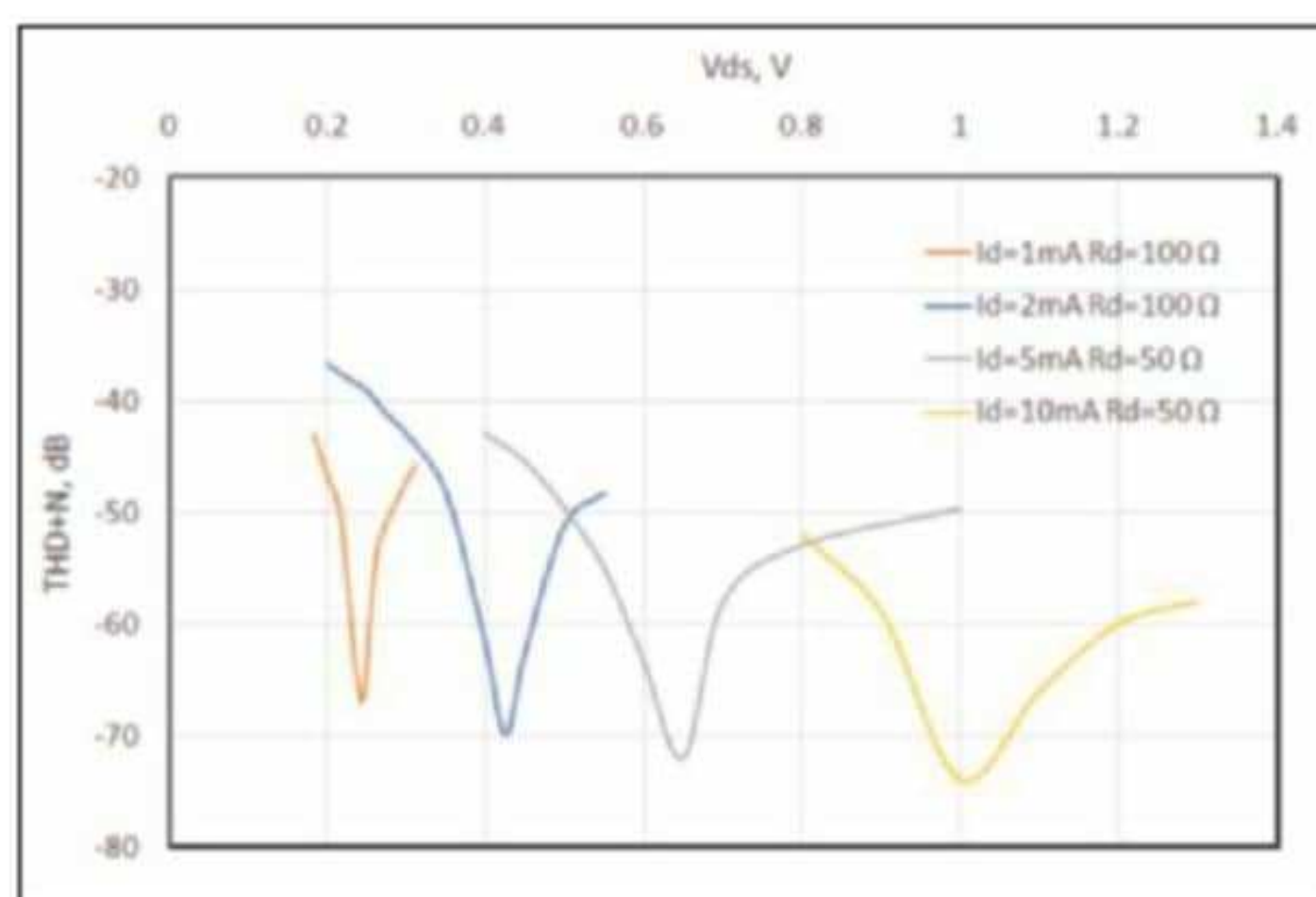


Figure 7: THD+N for CPH3910 JFET with variable  $V_{ds}$  and drain resistor. Input signal 10mV rms



minimums for each value of drain current. The minimums look a little bit narrower compared to the JFET cascode (Figure 5). At low drain to source voltages the nonlinearity in  $G_{os}$  of the device itself, reduced by  $R_d$  can compensate the quadratic nonlinearity of the JFET transfer for a certain range of the input signal  $v_{sig}$ . So, it is not necessary to use another JFET in common gate configuration to

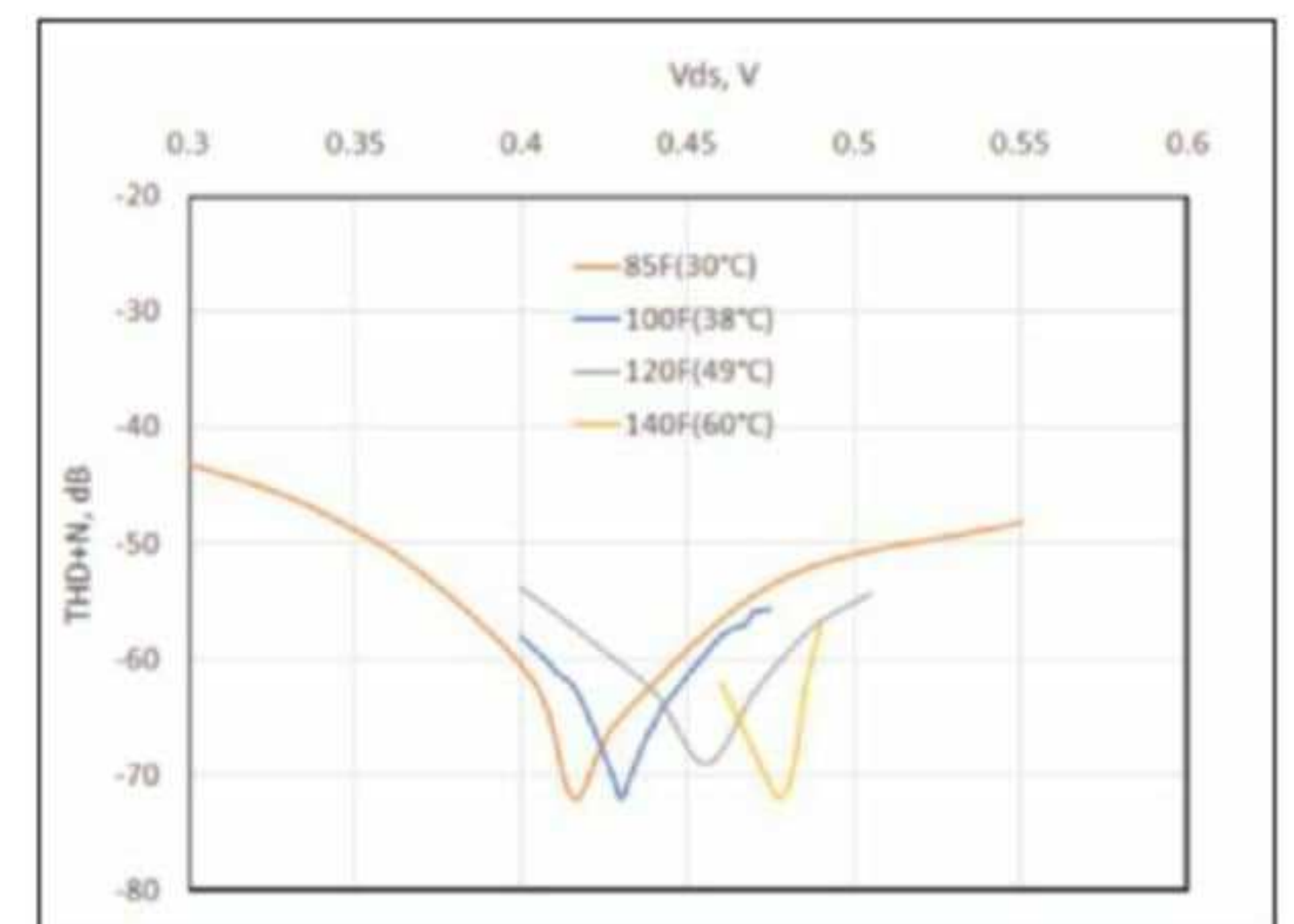


Figure 8: THD+N for CPH3910 JFET with variable  $V_{ds}$  with drain resistor  $R_d$ .  $R_d = 100\Omega$ . Input signal 10mV rms.

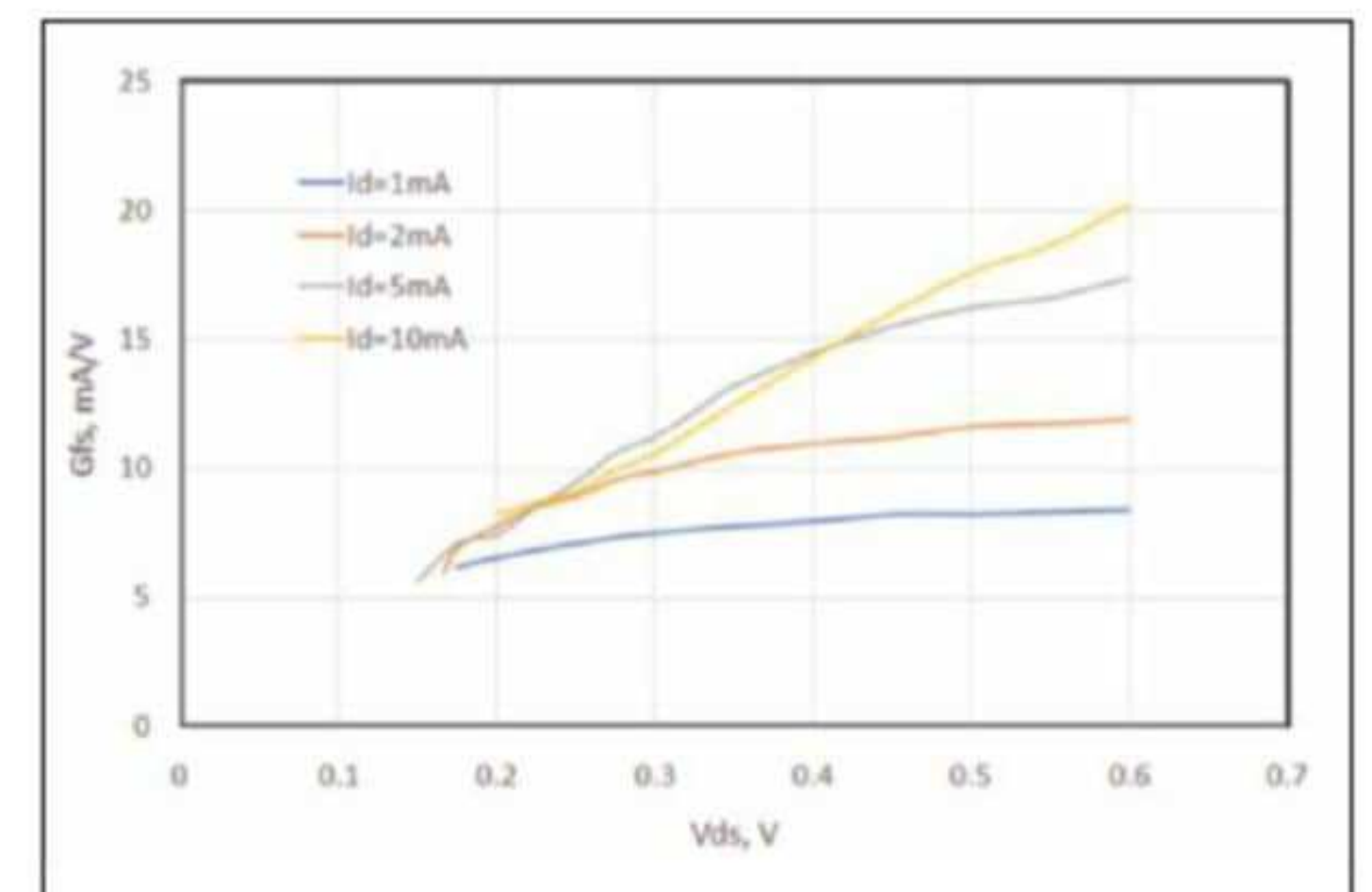


Figure 9: Transconductance curves for CPH3910 at low  $V_{ds}$

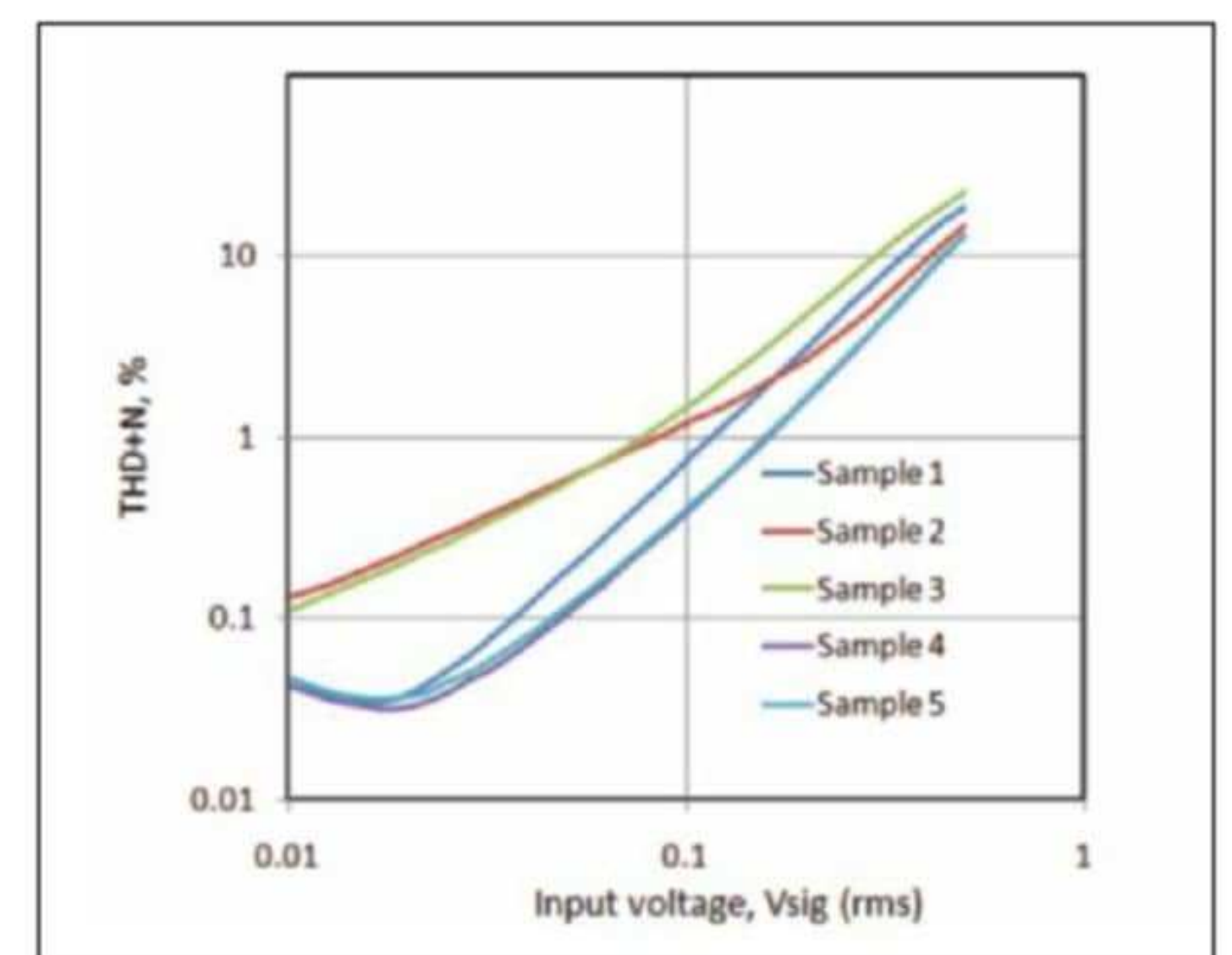


Figure 10: THD+N curves for different devices in the variable-resistance mode with a drain resistor and optimal  $V_{ds}$  (samples 1, 4, 5) and in saturation mode with high  $V_{ds}$  above the locus point (samples 2 and 3).



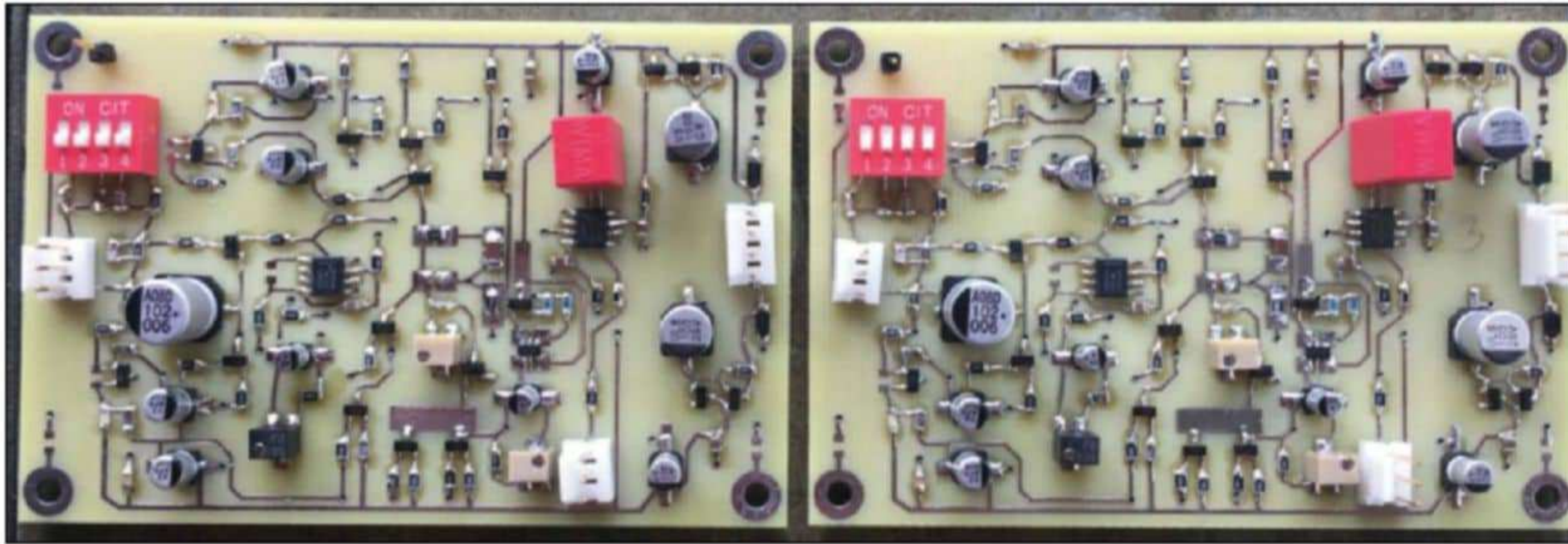


Photo 1: For the transconductance phono preamplifier, I built a practical circuit around JFETs in the variable resistance-mode with a drain load resistor.

achieve distortion compensation. The N nonlinear resistor also can be used in place of  $R_d$  (for example, JFET with  $V_{gs}=0$ ).

Now let me address the practical aspects of the JFET amplifying stage with a drain load resistor.  $V_{ds}$  should be maintained within a narrow range (say  $\pm 20\text{mV}$ ) to keep good distortion reduction (Figure 5 and Figure 7). How does this voltage depend on the device temperature? Temperature dependence of  $V_{ds}$  setting for minimum distortion is shown in **Figure 8**. The drain-source voltage for minimum distortion varies with temperature, however it is still possible to get substantial distortion reduction over an acceptable temperature range (in this case  $30^\circ\text{C} \dots 50^\circ\text{C}$ ) without  $V_{ds}$  trimming.

In the variable-resistance mode, transconductance  $G_{fs}$  strongly depends on the drain-source voltage. The thermal noise in the JFET channel can be modeled by a gate series resistance with the value  $R_n = 2/3G_{fs}$ . Its noise voltage can be calculated in the usual way  $E_n = \sqrt{4kTR_n}$ . If transconductance drops to half its value with  $V_{ds}$ , then the noise increases by 3dB.

Another important question comes to mind. Distortion reduction mentioned above is achieved for small input voltage 10mV rms. What is the distortion at high input signals? **Figure 10** illustrates distortion curves for the different devices with the same part number. Some JFETs have  $V_{ds}$  set near optimal value for minimum distortion, some of them have a high  $V_{ds}$  voltage. At low input level there is 15dB to 20dB improvement in distortion, and this improvement reduces with level. If we draw a line tangent to each curve and measure its slope, then we get a sense of the steepness. The slope of the THD curve for the devices in saturation region is about 1 (linear) and the slope for the THD curves for devices in the variable resistance-mode is about 2 (square). That means that a JFET in saturation mode produces mainly second-order harmonic while a JFET in the variable-resistance mode with drain resistor and optimum  $V_{ds}$  value produces mainly third-order harmonic.

This method for linearization of the JFET (MOSFET) transfer function can be used in the

circuits, which are optimized for single-ended amplifying devices and when the application of a differential pair is not straightforward.

Next, I will describe a practical circuit, built around JFETs in the variable resistance-mode with a drain load resistor (**Photo 1**).

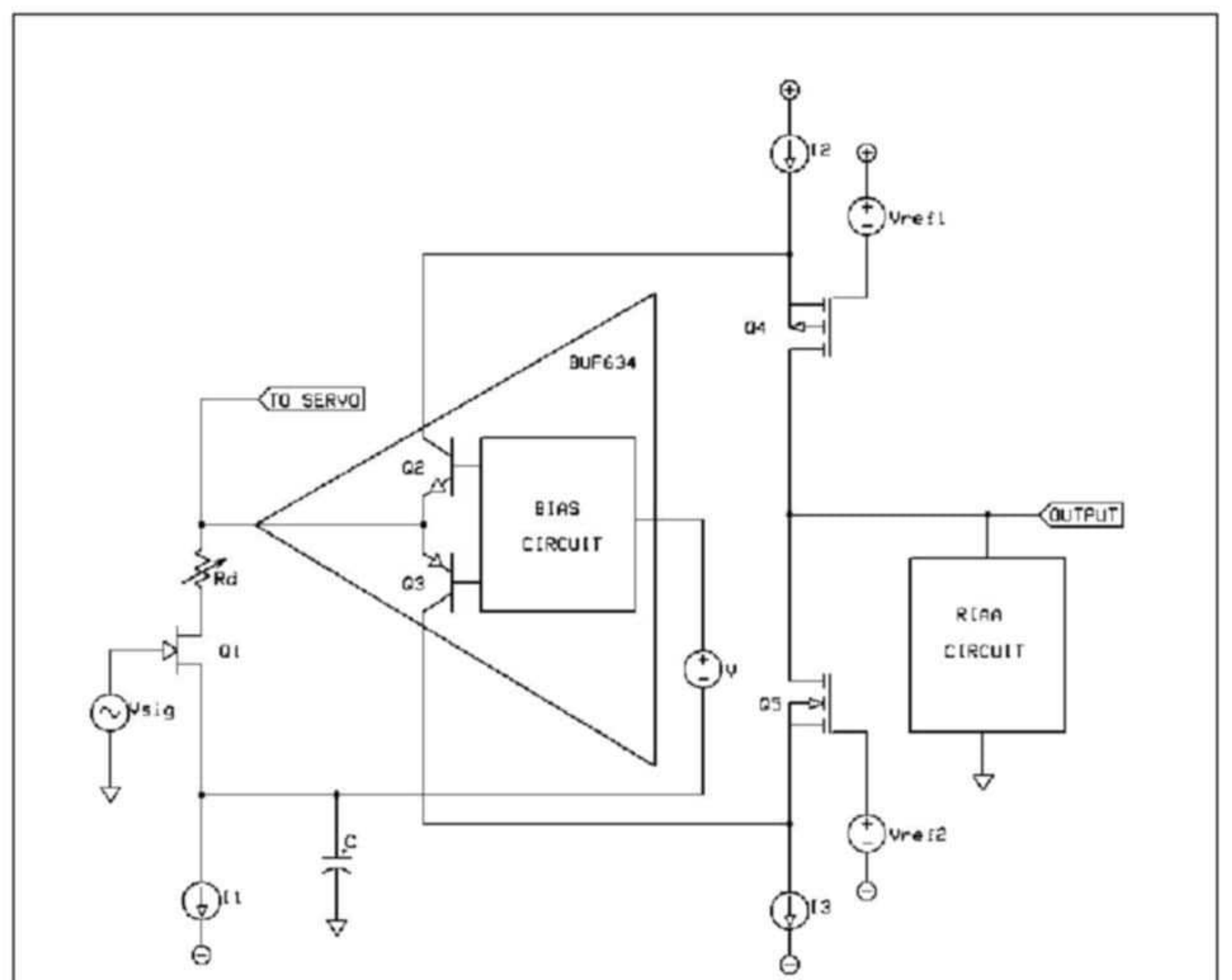


Figure 11: Simplified diagram of the transconductance phono stage

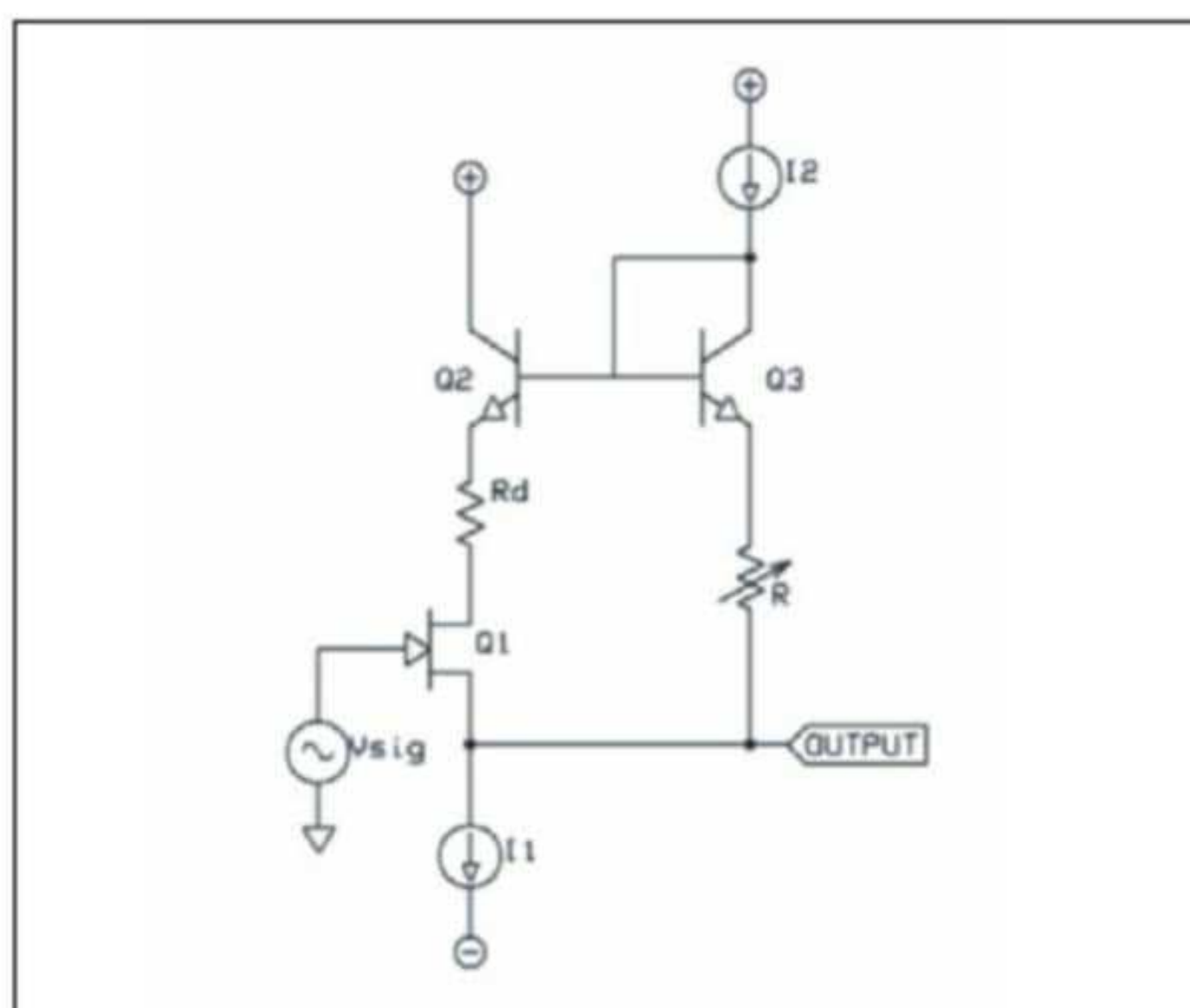


Figure 12: Simplified diagram of the output unity gain buffer



Figure 13: A fast Fourier transform (FFT) of distortion spectrum of standalone output unity gain buffer, shown in Figure 12. Load 100k $\Omega$ , output 1V rms, fundamental 1kHz.

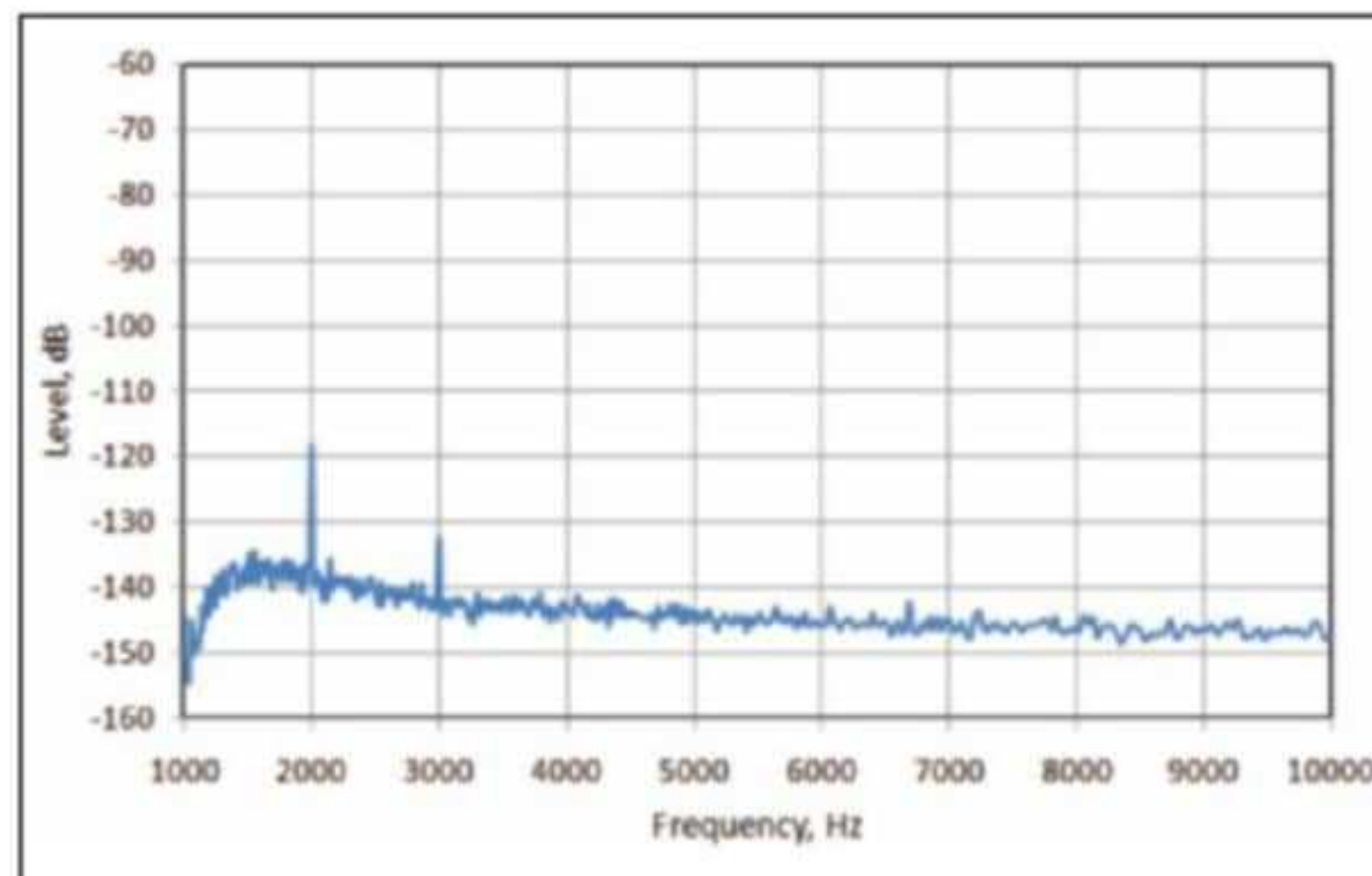
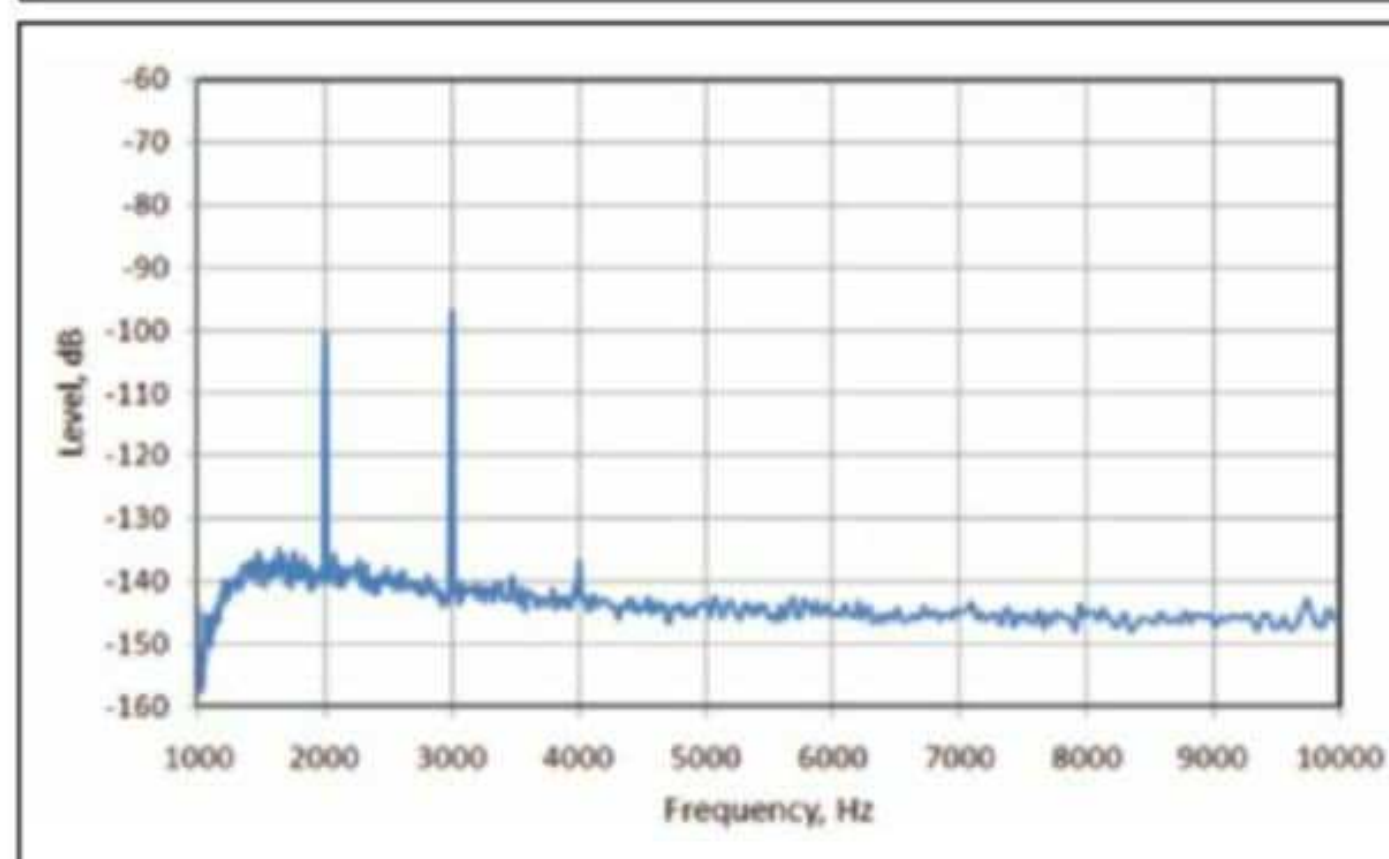


Figure 14: A FFT of distortion spectrum of standalone output unity gain buffer, shown in Figure 12. Load 600 $\Omega$ , output 1V rms, fundamental 1kHz.



## Transconductance Phono Preamplifier

Transconductance phono preamplifiers have been well known for years. I can mention the following designs (listed in random order): Dr Malcom Hawksford's circuits, Pink Triangle PIP phono by Owen Jones, Jonathan Carr's circuits, Creek OBH phono preamp by Alex Nikitin, Audio Interface Resources (AIR) preamplifier by Lars Clausen and John Madsen, and Paradise by Joachim Gerhard. These designs include a high transconductance amplifying stage loaded with a two-terminal RIAA network.

The amplifying stage output current passes through the RIAA network. The voltage across the RIAA network decreases with frequency according to the RIAA equalization curve. This voltage drop is limited only by amplifying stage peak output current. Transconductance phono preamplifiers usually have larger headroom (at least it is not limited by supply rail voltage).

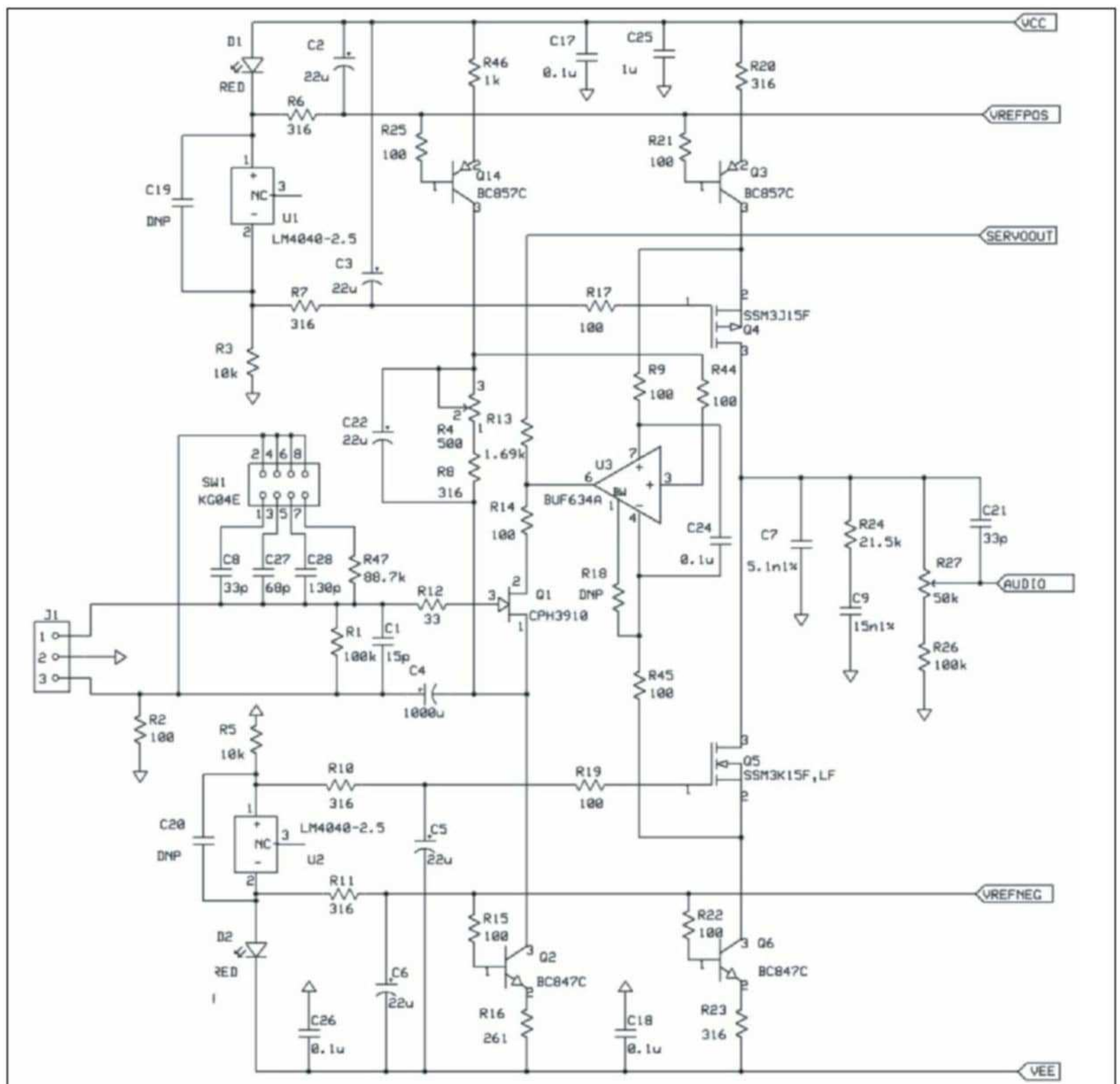


Figure 15: The full schematic of the transconductance phono preamp input stage and RIAA network



**The Circuit.** The basic topology is a zero global feedback concept based on a single amplifying JFET stage with current driven two terminal RIAA network as shown in **Figure 11**. Constant current source (CCS) I1 sets the operating point of the input common source stage (Q1) for 2mA. The input JFET has series drain resistor Rd. The output current of the input stage feeds the output terminal of the integrated buffer (BUF634A).

The floating voltage source together with the integrated unity gain buffer sets  $V_{ds}$  for the lowest distortion in the input stage. Output devices Q2, Q3 of the buffer transfer Q1 output current to the sources of the folded cascode stage (MOSFETs Q4 and Q5).

Current sources I2, I3 set the cascode devices quiescent current. The folded cascode stage has a high output impedance and is loaded with the CRCR RIAA two terminal network. The JFET unity

gain buffer shown in **Figure 12** isolates the RIAA network from the receiving equipment.

CCS I1 sets the operating point of the common drain stage (Q1) for  $I_d=20mA$ , the voltage across Q1 and Rd is equal to the voltage drop on trimmer R. This voltage drop is set by current source I2 and the value of the trimmer R. Trimmer R is adjusted for lowest distortion.

Transistor Q3 operates as a diode and compensates for the temperature variation of the base-emitter voltage of emitter follower Q2. The distortion spectrum of this unity gain buffer is shown in **Figure 13** and **Figure 14**. You can see that only the second and third harmonic are above the noise. This is remarkable performance for such simple circuit.

**Schematics.** The schematic of the complete transconductance phono preamplifier is shown in **Figure 15** and **Figure 16**. The preamp can be powered from a bipolar 15...18V supply. Red LEDs

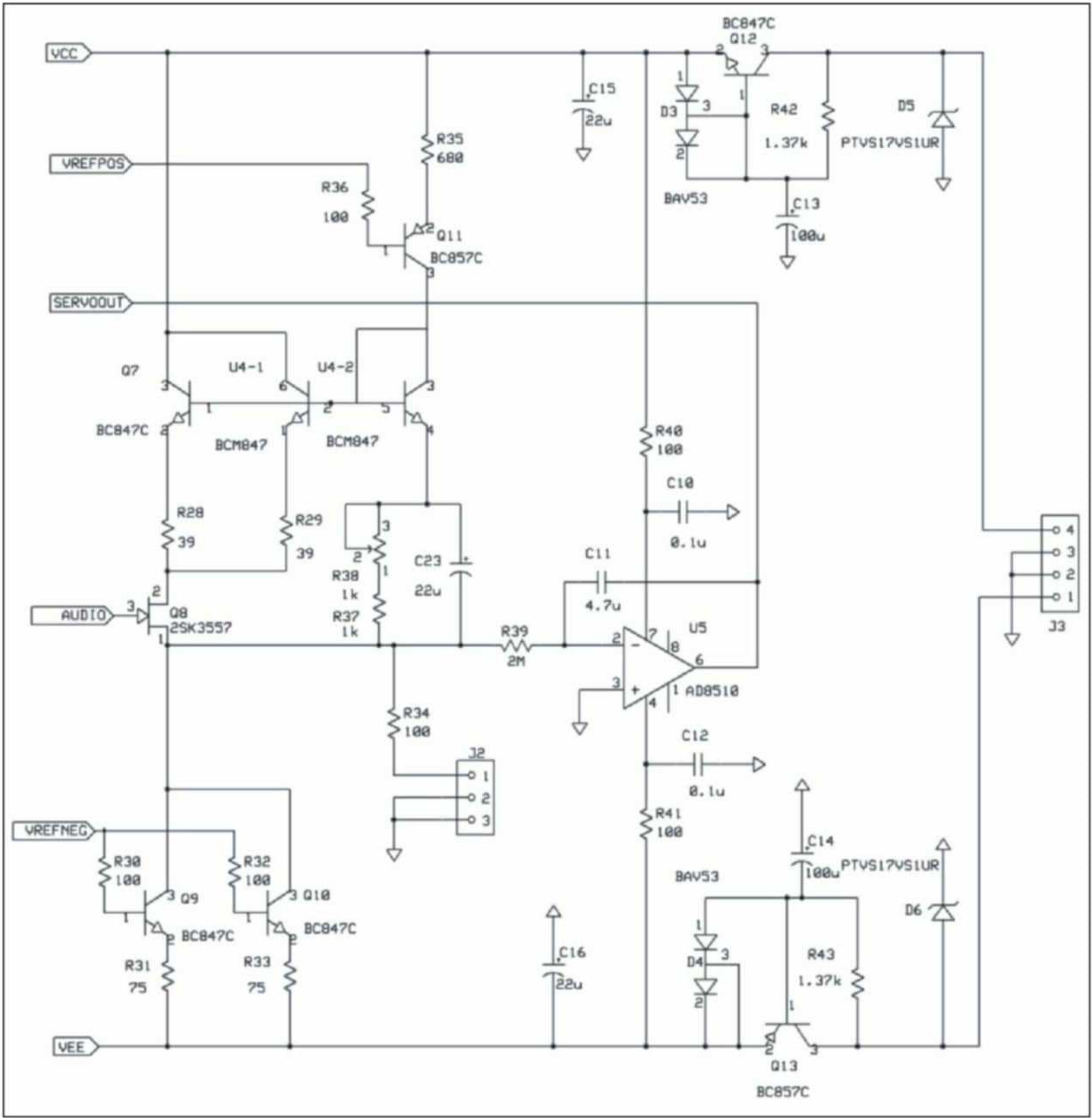


Figure 16: The schematic of the transconductance phono preamp output buffer



Figure 17: Frequency response of the transconductance phone preamplifier without RIAA equalization network components C7, C9, R24. Input JFET transconductance 6.7mA/V, load 150k $\Omega$  (R26+R27).

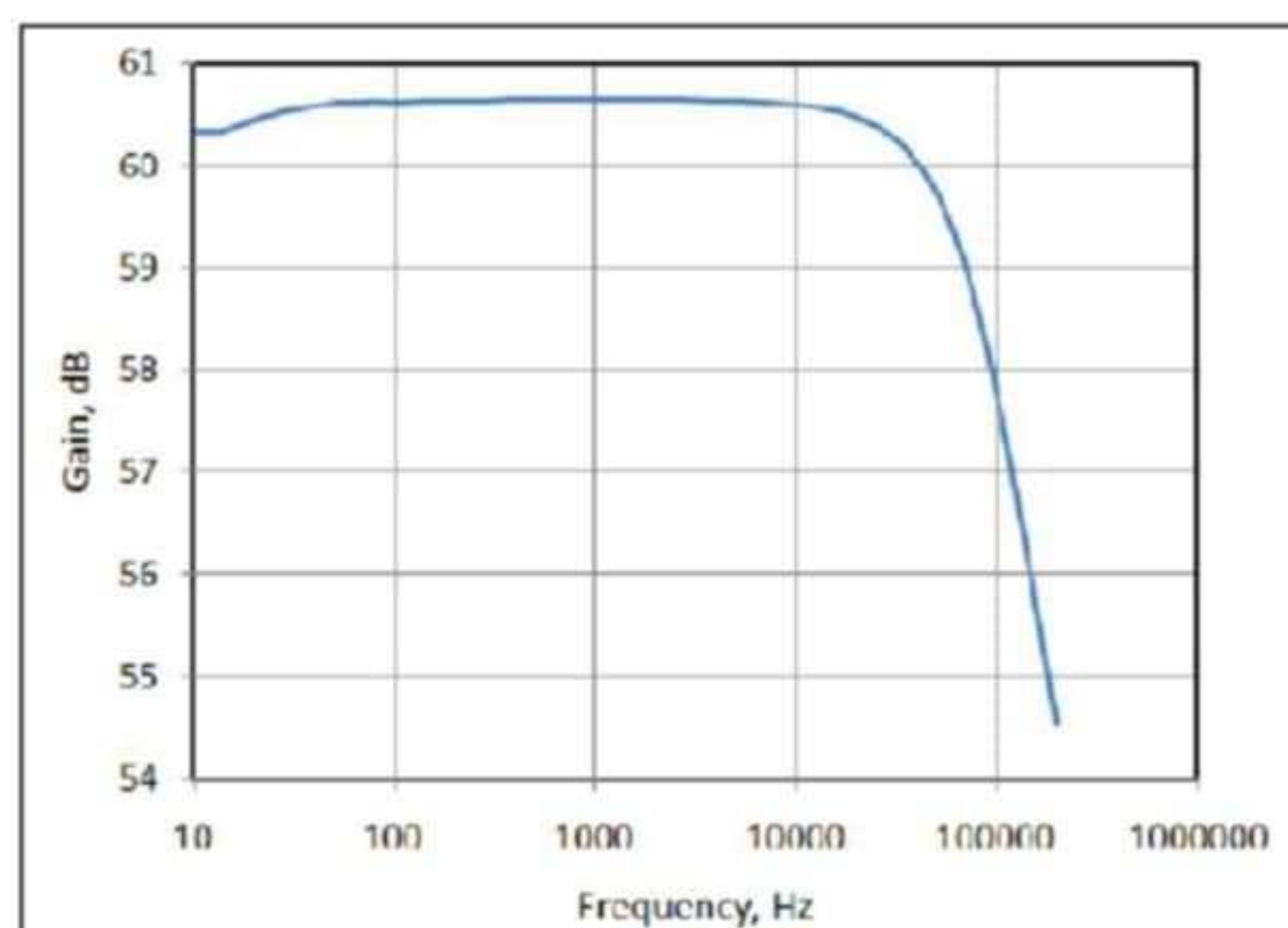


Figure 18: Deviation of the frequency response of the transconductance phone preamplifier from the RIAA curve

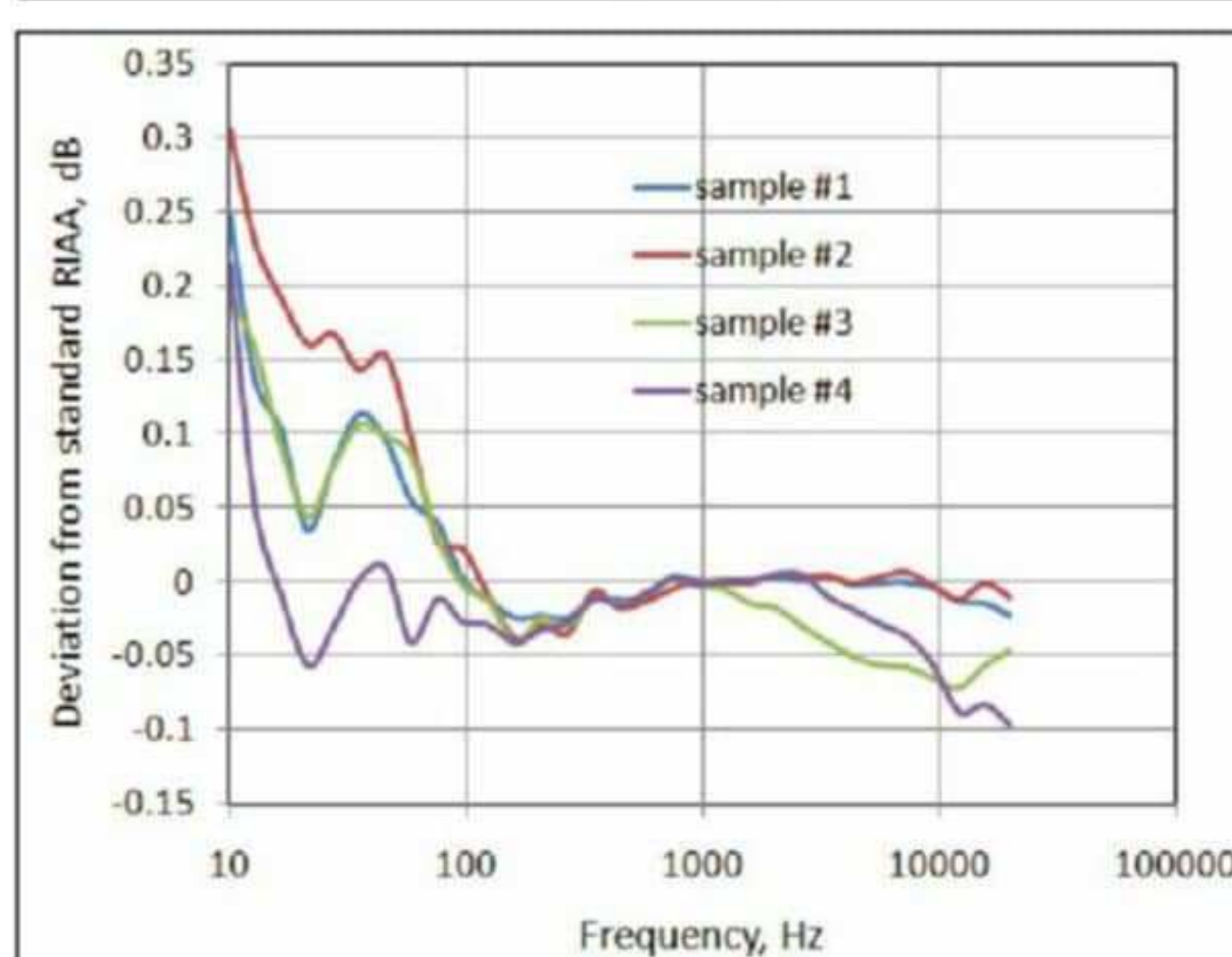


Figure 19: THD+N for the transconductance phono preamplifier for 1kHz and 6kHz sine wave, output voltage in Volts rms.

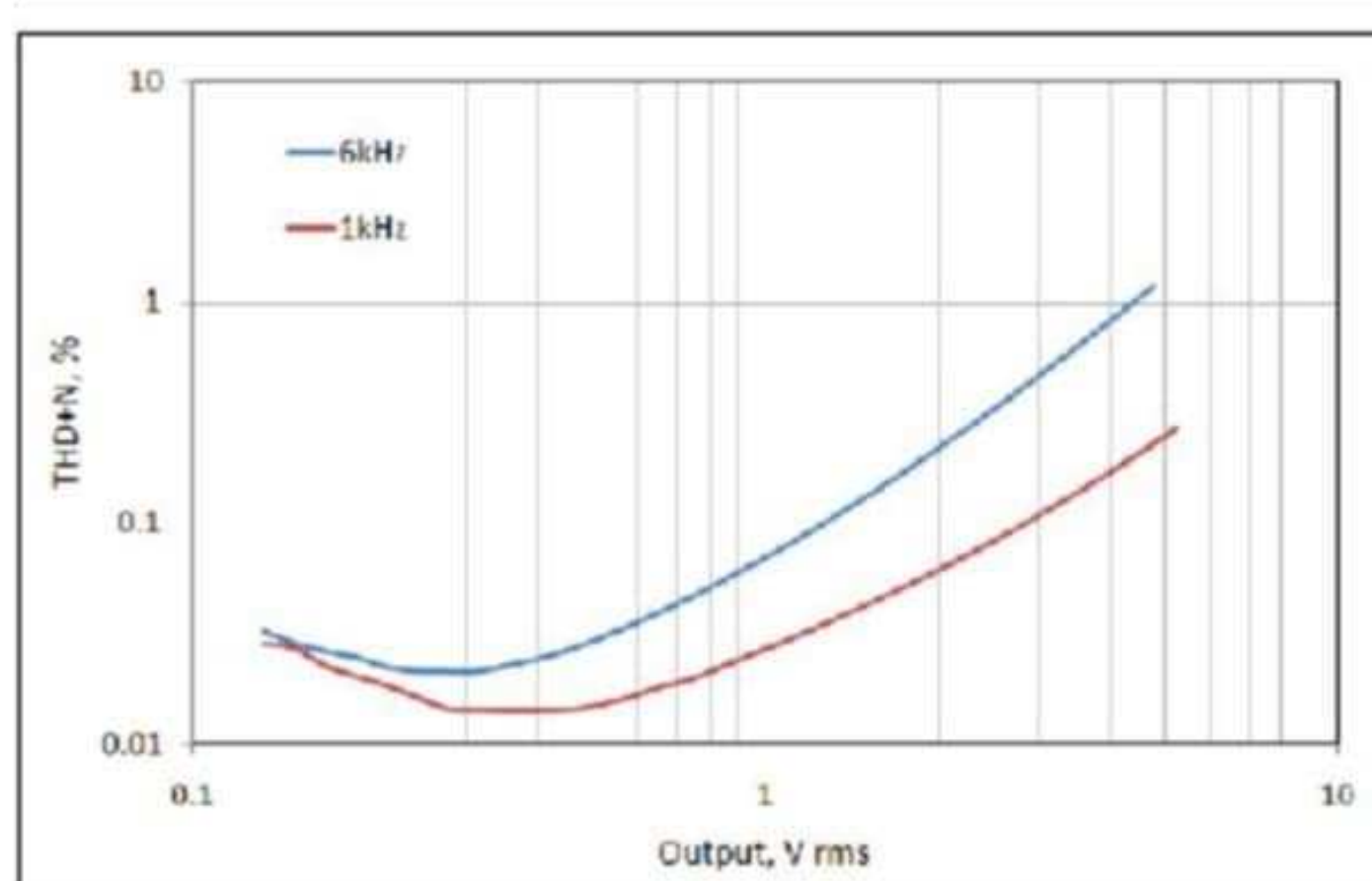
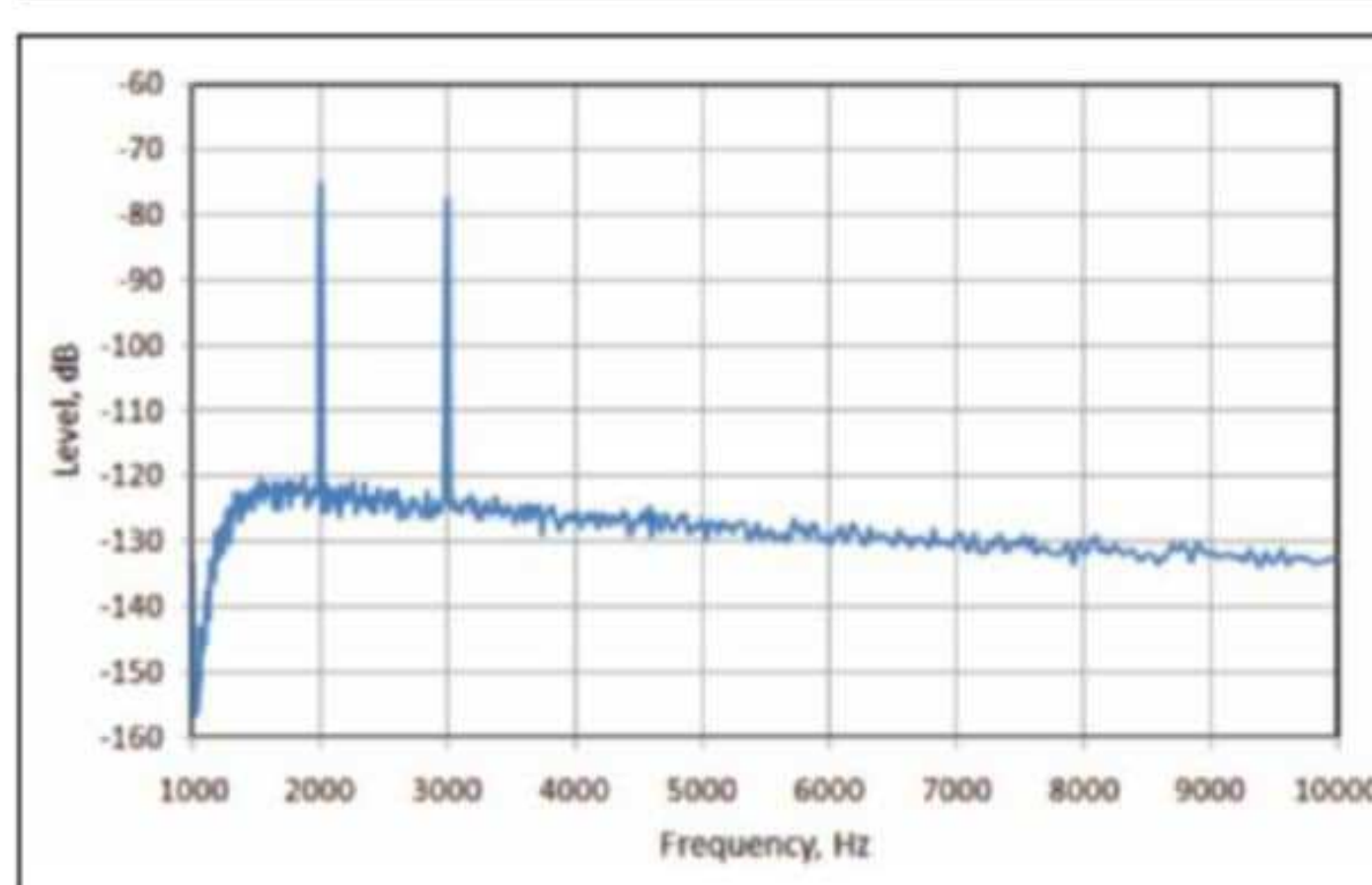


Figure 20. The FFT of the distortion spectrum for the transconductance phono preamplifier, output 1V rms, fundamental 1kHz



## About the Author

**Dimitri Danyuk** has been the principal hardware engineer at Harman luxury audio since 2013. He graduated with honors from Kyiv Polytechnic in 1985. His passion is to help audiophiles in all aspects of audio design. His articles have appeared in a number of magazines including *Journal of the Audio Engineering Society* (JAES), *IEEE Transactions*, *EDN*, *Electronic Design*, and more. Dimitri also provides consulting services for various businesses.



D1, D2 act as voltage references for the current sources Q2, Q6, Q9, Q10, Q14, Q3, Q11. Shunt voltage references U1, U2 provide gate voltage for the folded cascodes Q4, Q5. The reference voltages pass through corresponding low-pass RC filters. The MM pickup is connected between pins 1 and 3 of the input connector J1.

A ground lift switch can be connected to pins 2 and 3 of the same connector. DIP switch SW1 allows choosing different cartridge loads: 47k $\Omega$  and 100k $\Omega$ ; 33pF, 68pF, 100pF, 130pF, 160pF, 200pF, and 230pF. Q1 is the input JFET in common source configuration. Q1 works in variable-resistance mode with a small drain resistor R14. Q1 is the single amplifying device in the whole circuit. Trimmer R4 sets the voltage between drain and source. Integrated open-loop buffer U3 passes Q1's output current to the sources of cascode devices Q4, Q5. The MOSFETs are chosen as cascode devices due to their low output transconductance. The folded cascode stage is loaded with a CRCR RIAA two terminal network. Trimmer R27 allows altering the total gain within  $\pm 1.5$ dB to compensate for Q1 transconductance spread.

A source follower Q8 isolates the load from the high impedance RIAA network. There are two current sources in the source network (Q9, Q10) to keep device dissipation within limits. There are also two paralleled drain devices (Q7, U4-1) for the same reason. Trimmer R38 sets the voltage drop between the source follower source and drain. The load is connected at J2. Inverting integrator U5 provides the necessary DC voltage to the first stage. There is a capacitance multiplier filter in each power rail (Q12, Q13) for removing power supply residual hum. Transient voltage suppressors D5, D6 protect from overvoltage and reverse power. Schematics and PCB files, the BOM and Gerber files for the preamplifier can be found in the Supplementary Materials section of the *audioXpress* website.

**Test Results.** The measurement results of the complete phono preamp are shown in **Figures 17–21**. The noise level (60dB gain, no RIAA network) is 360 $\mu$ V in a 22kHz BW or 2.5nV/ $\sqrt{\text{Hz}}$ .

**Adjustment.** The adjustment is simple—set minimum distortion at low output level (100mV) by trimmer R4, set minimum distortion at higher output level (1V) by trimmer R38, make the output signals equal with trimmer R27.

## Conclusion

Further improvements are possible. The distortion is limited by the performance of the input stage. Distortion can be reduced by setting the drain current in the first stage to a higher value.